Please replace the Abstract with the following new Abstract:

An integrated circuit inductor includes a spiral pattern disposed upon a substrate. The track of the spiral is divided into multiple tracks to form a multi-track inductor. The individual tracks are disposed side by side and in different layers. Tracks that are aligned vertically are coupled by feed throughs, or vias. Multiple vias are used along the length of each of the multiple tracks. Tracks disposed in the same layer are joined together at their beginning, and at their termination. A patterned shield is fabricated from conductive fingers of n+ salicided material that is separated by non conducting polysilicon that fills the gaps between the fingers. The conductive fingers are coupled together in groups, which are in turn tied to a single point ground. In tying the groups together, a gap in the conducting path is provided to prevent ground loop currents. The shield is disposed between the multi-track inductor and the substrate.

In the Specification:

On page1, please replace the paragraph starting on line 10, with the following:

This application is a continuation-in-part of patent application entitled "System and Method for ESD Protection," by Agnes N. Woo, Kenneth R. Kindsfater, and Fang Lu, filed January 14, 2000, U.S. Patent Application No. 09/483,551; which is a continuation-in-part of U.S. Patent Application No. 09/439,101 filed November 12, 1999; the disclosures of which are incorporated herein by reference.

On page 80, please replace the paragraph starting on line 15, as follows:

FIG. 32 shows a transconductance stage 3102 with an LC load 3104 that is provided with Q enhancement 3202 and Q compensation over temperature 3206. Q enhancement 3202 tends to increase the circuit Q thus, increasing the frequency selectivity of the circuit. A Q enhancement is provided by the transconductance element's G_m 3202 connected as shown. Addition of this transconductance element is equivalent to adding a negative resistance 3024 that is temperature dependent in parallel with R'(T). This negative resistance tends to cause cancellation of the parasitic resistance thus, tending to increase the circuit Q. The details of Q enhanced filters are disclosed in more detail in U.S. Patent Application No.09/573,356, filed 5/17/00 entitled, "New CMOS Differential Pair Linearization Technique" by Haideh Khorramabadi; based on U.S. Provisional Application